

CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test (Frontiers in Electronic Testing)

By Andrei Pavlov, Manoj Sachdev

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The monograph will be dedicated to SRAM (memory) design and test issues in nano-scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues. Purpose: provide process-aware solutions for SRAM design and test challenges.

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Editorial Review

From the Back Cover

As technology scales into nano-meter region, design and test of Static Random Access Memories (SRAMs) becomes a highly complex task. Process disturbances and various defect mechanisms contribute to the increasing number of unstable SRAM cells with parametric sensitivity. Growing sizes of SRAM arrays increase the likelihood of cells with marginal stability and pose strict constraints on transistor parameters distributions.

Standard functional tests often fail to detect unstable SRAM cells. Undetected unstable cells deteriorate quality and reliability of the product as such cells may fail to retain the data and cause a system failure. Special design and test measures have to be taken to identify cells with marginal stability. However, it is not sufficient to identify the unstable cells. To ensure reliable system operation, unstable cells have to be repaired.

CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies covers a broad range of topics related to SRAM design and test. From SRAM operation basics through cell electrical and physical design to process-aware and economical approach to SRAM testing. The emphasis of the book is on challenges and solutions of stability testing as well as on development of understanding of the link between the process technology and SRAM circuit design in modern nano-scaled technologies.

About the Author
Prof. Sachdev has authored several successful books with Springer

Users Review

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