

Microarchitecture of Network-on-Chip Routers: A Designer's Perspective

By Giorgos Dimitrakopoulos, Anastasios Psarras, Ioannis Seitanidis

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This book provides a unified overview of network-on-chip router micro-architecture, the corresponding design opportunities and challenges, and existing solutions to overcome these challenges. The discussion focuses on the heart of a NoC, the NoC router, and how it interacts with the rest of the system. Coverage includes both basic and advanced design techniques that cover the entire router design space including router organization, flow control, pipelined operation, buffering architectures, as well as allocators’ structure and algorithms. Router micro-architectural options are presented in a step-by-step manner beginning from the basic design principles. Even highly sophisticated design alternatives are categorized and broken down to simpler pieces that can be understood easily and analyzed. This book is an invaluable reference for system, architecture, circuit, and EDA researchers and developers, who are interested in understanding the overall picture of NoC routers' architecture, the associated design challenges, and the available solutions.

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Editorial Review

From the Back Cover

This book focuses on the microarchitecture of network-on-chip routers from a designer’s perspective, providing ready-to-use solutions for simple and more sophisticated design cases. All aspects of the design of a network-on-chip router, including flow control, buffering architectures, arbitration and allocation, as well as pipelined organizations, are presented in detail. The authors provide numerous detailed examples and practical abstract models, when necessary. Router micro-architectural options are presented in a step-by-step manner, beginning from basic design principles. Even highly sophisticated design alternatives are categorized and broken down to simpler pieces that can be understood easily and analyzed. This book is an invaluable reference for system, architecture, circuit, and EDA researchers and developers, who are interested in understanding the overall picture of network-on-chip routers' microarchitecture, the associated design challenges, and the available solutions.

· Covers all aspects of the microarchitecture of Network-on-Chip routers;

· Justifies and explains every design choice that is presented in a ready-to-use manner following a designer’s perspective;

· Describes performance-enhancing features in a step-by-step manner;

·Includes detailed examples presenting the flow of information inside the router on a cycle-by-cycle basis, highlighting the operation of each part under regular or worst-case traffic scenarios.

Users Review

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Katherine Anderson:

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